REMARKS

Applicants appreciate the time taken by the Examiner to review Applicants' present application. This application has been carefully reviewed in light of the Official Action mailed February 26, 2004. Applicants respectfully request reconsideration and favorable action in this case.

Rejections under 35 U.S.C. § 112

Claims 15 and 21-27 stand rejected under 35 U.S.C. § 112, second paragraph. Applicants have amended Claims 15 and 25 to removed the term "skip" or "skipped". With respect to "more slowly" and "more quickly." Applicants submit that the fact that claim language, including terms of degree, may not be precise, does not automatically render the claim indefinite under 35 U.S.C. 112 second paragraph. Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification. *See* MPEP 2173.05(b). Claim 21 recites determining whether "read logic is reading data out of the circular buffer more quickly or more slowly than the write logic is writing data into the circular buffer." One of ordinary skill in the art would understand that if the read logic is reading data out of the circular buffer more quickly than the write logic is writing data to the buffer, then data is leaving the buffer faster than it is being stored to the buffer. If, on the other hand, the read logic is reading data out of the circular buffer more slowly than the write logic is writing data to the buffer, then data is being written to the buffer more quickly than data is leaving the buffer. Applicants believe that the concept of reading data "more quickly" or "more slowly" than writing data would be understood, regardless of the precise speeds at which data is read from the buffer or written to the buffer. Therefore, Applicants believe that the terms "more slowly" and "more quickly" are not indefinite and request withdrawal of the rejections.

Rejections under 35 U.S.C. § 103

Claims 1, 12, 13, 21, 22, 24, 26 and 27 stand rejected as obvious over U.S. Patent No. 6,289,066 ("LaVigne"). In regard to the these rejections, the Examiner states:

> LaVigne discloses a system and method to retime signals between input and output signals running at different rates comprising . . . comparing the read and write pointers to determine a number of storage location by which the write pointer leads the read pointer (col. 5: lines 3-26) . . . overwriting one of

> the storage locations in response to detecting that the number of storage locations by which the write pointer leads the read pointer is greater than a predetermined maximum number (col. 5 lines 12-26; fig 2 delete region 30).

Applicants note that in order to establish a prima facie case of obviousness, the Examiner must show: that the prior art references teach or suggest all of the claim limitations; that there is some suggestion or motivation in the references (or within the knowledge of one of ordinary skill in the art) to modify or combine the references; and that there is a reasonable expectation of success. M.P.E.P. 2142, 2143; In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). The Examiner must explain with reasonable specificity at least one rejection – otherwise, the Examiner has failed procedurally to establish a prima facie case of obviousness. M.P.E.P. 2142; Ex parte Blanc, 13 U.S.P.Q.2d 1383 (Bd. Pat Application. & Inter. 1989). When the motivation to combine the teachings of the references is not immediately apparent, it is the duty of the Examiner to explain why the combination of the teachings is proper. Ex parte Skinner, 2 U.S.P.Q.2d 1788, 1790 (Bd. Pat. App. & Inter. 1986). Applicants respectfully submit that the Examiner has not made out a prima facie case of obviousness as the Examiner has not shown where the prior art references teach or suggest each of the Claim limitations.

Claim 1 of the present invention recites "comparing the read and write pointers to determine a number of storage locations by which the write pointer leads the read pointer . . . overwriting one of the storage locations in response to detecting that the number of storage locations by which the write pointer leads the read pointer is greater than a predetermined maximum number" and Claim 12 of the present invention recites "determining a number of storage locations by which the write pointer leads the read pointer . . . and overwriting one of the storage locations which contains a fill word one or more times in response to detecting that the number of storage locations by which the write pointer leads the read pointer is greater than a predetermined maximum number." Each of these claims share the features that the difference in the positions of the read pointer and write pointer can be determined and, if it is determined that the write pointer leads the read pointer by a particular amount, a storage location can be overwritten.

Claim 13 recites "control logic configured to compare the positions of the read and write pointers and configured to control the write logic to adjust the write pointer in response to the relative positions of the read and write pointers." In claim 13, the position of the write pointer can be controlled based on the relative position of the read and write pointers.

Claim 21 recites "control logic configured to determine whether the read logic is reading data out of the circular buffer more quickly or more slowly than the write logic is writing data into the circular buffer, and if the read logic is reading data out of the circular buffer more quickly than the write logic is writing data into the circular buffer, modify the position of the read pointer; and if the read logic is reading data more slowly than the write logic is writing data into the circular buffer, the control logic is configured to modify the position of the write pointer to compensate therefore." In Claim 21, the position of the write pointer can be controlled based on the relative difference in the speeds with which data is written to/read from the buffer.

Col. 5, lines 3-26 of LaVigne describe a system of adding or removing data from a FIFO. The buffer is divided into several sections--"add", "neutral" and "delete"--based on the amount of data in the buffer relative to the buffer capacity (i.e., based on whether the buffer is less than half full, half full, or more than half full). If the buffer is less than half full and the insert pointer is in the read region and the "I", "J", "K" and "L" elements are "Idle" or "Config" symbols, the extract pointer "holds after a bank 0 read, thus replicating elements 'I' and 'J'." *See* col. 5, lines 3-11. If on the other hand, the insert pointer is in the "delete" region, and the "I", "J", "K" and "L" elements are "Idle" or "Config" symbols, "the extract pointer clocks ahead after the bank 1 read, as well as after the bank 0 read." *See* col. 5, lines 4-26.

Thus, the portion of LaVigne cited by the Examiner teaches that based on the position of the write pointer in the buffer, the behavior of the extract pointer is modified to either replicate symbols (i.e., replicate "I" and "J") or skip symbols (i.e., "J" and "K"). Applicants, however, submit that there is no teaching or suggestion in the portions of LaVigne cited by the Examiner to overwrite a storage location in response to detecting that the number of storage locations by which the write pointer leads the read pointer is greater than a predetermined maximum number as recited in independent Claim 1 and 12. Moreover, there is no teaching or suggestion in the portions of LaVigne cited by the Examiner to control the write logic to adjust the write pointer in response to the relative positions of the read and write pointers as recited in independent Claim 13 nor is there a teaching or suggestion to modify the position of the write pointer to compensate for the fact that "the read logic is reading data out of the circular buffer more quickly than the write logic is writing data into the circular buffer" as recited in independent Claim 21. Applicants, therefore submit that Lavigne does not teach or suggest each element of independent claims 1, 12, 13 and 21. Applicants therefore request allowance of Claims 1, 12, 13 and 21. Additionally, Applicants request allowance of Claims 2-11 as depending on Claim 1, 14-20 as depending on Claim 13 and 22-27 as depending on Claim 21.

Applicants have now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-27. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-0456 of Gray Cary Ware & Freidenrich, LLP.

Respectfully submitted,

Gray Cary Ware & Freidenrich LLP
Attorneys for Applicants

John L. Adair
Reg. No. 48,828

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1221 South MoPac Expressway, Suite 400
Austin, TX 78746-6875
Tel. (512) 457-7142
Fax. (512) 457-7001